Amendments to the Specification

Please replace the title on page 1, lines 1 to 2 with the following:

~~AN ANALOG-TO-DIGITAL CONVERSION ARRANGEMENT, A METHOD FOR ANALOG-TO-DIGITAL CONVERSION AND A SIGNAL PROCESSING SYSTEM, IN WHICH THE CONVERSION ARRANGEMENT IS APPLIED~~ ANALOG-TO-DIGITAL CONVERTER HAVING INTERLEAVED COARSE SECTIONS COUPLED TO A SINGLE FINE SECTION

Please replace the paragraph beginning on page 2, line 9 with the following:

Although various types of coarse and fine analog-to-digital converters can be used, for example flash analog-to-digital converters, in a particular embodiment these coarse and/or fine resolution analog-to-digital converters are formed by successive approximation analog-to-digital converters. It is possible to form the coarse resolution converters by flash converters and the fine resolution converter by a successive approximation converter; although flash converters ~~has~~ have the disadvantage that they need more circuit blocks, they have the advantage that more bits can ~~de~~ be determined at the same time in the same clock period, while in successive approximation converters more clock periods are necessary to determine the successive bits. Also it is possible to apply successive approximation converters as coarse resolution converters and a flash converter as the fine resolution converter.

Please replace the paragraph beginning on page 4, line 11 with the following:

In a more simplefonn the successive approximation analog-to-digital converter operates without so called overranging. This means that the voltage range for the determination of a bit value is divided in only two separated regions and by means of a single comparator unit is determined in which region the sample voltage value lies, which region again is

divided into two separated regions and so on. However, as will be explained hereinafter, for a coarse analog-to-digital conversion the application of overranging is favorable. This means that the voltage range for the determination of a bit value is divided in overlapping regions, particularly three regions, and by means of more comparator units is determined whether the sample voltage value lies only in one of the outmost voltage regions or in more than one voltage region. In the present application it will be supposed that, in the case of overranging, the voltage range of the sample input value is divided into three regions, so that the comparator 5 in that case may comprise two comparator units. Based upon the comparison results a chosen region is again divided into three regions, and so on. Instead of two comparator units it is possible to use only one comparator and to perform the two comparison actions one after the other; in that case the conversion needs more time. In general overranging makes it possible to determine more bits at the same time; this mean that overranging includes some aspects of flash conversion.

Please replace the paragraph beginning on page 5, line 20 with the following:

Now, with reference to Fig. 2b, the conversion with overranging, in this example three overlapping voltage ranges, will be explained. In a first step the digital control unit 7 generates two signals, viz.0110 and 1010, corresponding with 3/8 V and 5/8 V. The comparator 5 in this example comprises two comparator units. In the first comparator unit the sample input value V ; is compared with 3/8 V and in the second comparator unit with 5/8 V. As shown in Fig. 2b, Vi > 5/8 V, with the consequence that by both comparator units a value "1"is supplied to the digital control unit 7. During the conversion process bits are generated which are rounded off later on; in the digital values these bits are indicated by bits behind a "point". Based on the latter comparator output signals"1, 1", a starting value 0000.0 of the digital output signal is changed into 1000.0 by a full adder operation of both"l's"to the second"0"of the starting value; with this operation the first bit of the analog-to-digital conversion is determined. As both comparator units supplied asignal"1", the most upper region is selected for comparison purposes during the second step. In the second step, in the digital control unit the next

two comparator values are determined, viz.1011 and1101, corresponding with 11/16 and 13/16 V, lying in the upper region. As V ; < 11/16, by both comparator units avalue"0"is supplied to the digital control unit 7. By means of a full adder operation of both"0's'9 on thethird"0"of the value 1000.0, the secondbit 0 of the analog- to-digital conversion is determined. As both comparator units supplied asignal'40", the most lower region is selected for comparison purposes during the third step. In the third step, in the digital control unit the next two comparator values are determined, viz.1001. 1 and1010. 1, corresponding with 19/32 and 21/32. As shown in Fig. 2b,V ; > 21/32, with the consequence that again by both comparator units a value"1"is supplied to the digital control unit. By means of a full adder operation ofboth"1's"on the fourth"0"of the value 1000.0, the third bit of the analog-to-digital conversion is determined; the value 1000.0 is changed into 1010.0. In the fourth step, in the digital control unit the next two comparator values are determined, viz.1010. 11 and 1011. 01, corresponding with 43/64 and 45/64. NowV ; > 43/64 andV ; < 45/64, with the consequence that the first comparator unit supplies avalue"1"to the digital control unit 7 and the second comparator unit a value"0". By means of a full adder operation of the values"1"and"0"on the fifth"0"of the value1010. 0 the fourth bit of the analog-to- digital conversion is determined; the value1010. 0 is changed into1011. 0. As in the present example the conversion is performed in four bits, the conversion result is rounded off and again 1011, whereafter a next sample conversion can be started.

Please replace the paragraph beginning on Page 6, line 11with the following:

Although in this case there is no difference in the conversion result between the conversion without overranging and with overranging, differences may occur when, without overranging, the settling time for the voltages at the entrance of the comparator during transitions between two successive sample voltage values or two successive value of the digital-to-analog converter is too long, taking into account a desired sample rate. As the output resistance of the buffer amplifier 1 and the ~~capacity~~ capacitance of the capacitor 4, which is mostly a parasitic ~~capacity~~ capacitance, can difficultly be adjusted,

the settling constant of the sample voltage value is practically a given one. When there are great differences between two successive sample voltage values, the time necessary to approach the new sample voltage value may be unsatisfactory at a given sample rate. To decrease the sample rate, however, is mostly undesired. Also at the output of the digital converter 6 offset values or a too long settle time may occur. In those circumstances the values at one or both sides of the comparator may be incorrect.

Please replace the paragraph beginning on Page 7, line 21with the following:

Not only by overranging, but also by the application of interleaving the sample rate can be made higher. Interleaving implies a parallel conversion of successive sample voltages. In the present invention interleaving is only applied for the coarse resolution conversion. Although a number of parallel coarse resolution conversion channels ~~is~~ are applied, according to the invention they all make use of the same fine resolution analog-to-digital converter. By applying the same converter for the least significant part of the digital output signal, the effect of possible offset differences between the parallel coarse resolution conversion channels can be eliminated. The more expensive and power consuming fine resolution converter is applied for all the conversion channels. A basic block diagram for the complete analog-to-digital conversion arrangement according to the invention is indicated in Fig. 4. This arrangement gives an implementation of the combinationof : interleaved coarse resolution analog-to-digital converters; and one single fine resolution analog-to-digital converter.

Please replace the paragraph beginning on Page 9, line 21 the following:

In this preferred embodiment, for coarse resolution conversion two digital-to-analog converters 15a and 15b are sufficient. During phases 2 and 3 the switch 18a is in the position, indicated in Fig. 5: analog comparator signals are supplied to comparator

14a. During phases 3 and 4 the switch 18b is in the position, indicated in Fig. 5: analog comparator signals are supplied to comparator 14b. During phases 4 and 5 the switch 18a is in the position, different from that in Fig. 5: analog comparator signals are supplied to comparator 14c. During phases 5 and 6 the switch 18b is in the position, different from that in Fig. 4: analog comparator signals are supplied to comparator 14d. Of course it is possible to use four 8-bits digital-to-analog converters ~~in stead~~ instead of the two converters 15a and 15b with switches 18a and 18b.

Please replace the paragraph beginning on Page 10, line 25 the following:

The embodiment of the present invention described herein is intended to be taken in an illustrative and not limiting sense. Various modifications may be made to ~~these~~ this embodiment by persons skilled in the art without departing from the scope of the present invention as defined in the appended claims. For instance, the coarse as well as the fine resolution conversion can be performed for 6 bits, again resulting in a12 bits conversion. In that case the conversion time can be divided in three phases, each during 6 clock pulses, one for sampling and hold, a second for coarse resolution conversion and a third for fine resolution conversion, so that three interleaving channels can be used. Of course, conversion in a different number of bits is possible.